Agilent E9526A IBM PowerPC 4xx Trace Port Decoder and Inverse Assembler

Design Guide

Agilent Technologies

Notices

Manual Part Number

E9526-97000

This manual is available online at www.agilent.com. It is not an orderable part.

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1 Introduction

In This Guide...

This *Design Guide* provides information to assist you in designing a board which will be compatible with the Agilent E9526A IBM PowerPC 4xx Trace Port Decoder and Inverse Assembler. It tells you what signals are required by the decoder, and suggests how to route these signals to a connector.

For information on using the decoder, see the online help which is installed with the decoder.

Product Overview

The IBM PowerPC 4xx Trace Port Decoder and Inverse Assembler, used with an Agilent Technologies logic analyzer, allows you to decode and view trace port messages from an IBM PowerPC 4xx processor core in your target system. Processor execution is disassembled and displayed as assembly language mnemonics.

Target System Requirements

The inverse assembler has been designed to work with target systems meeting the following requirements:

Supported processor

- The initial version of this product supports the IBM PowerPC 405 processor core.

Object files

- You must have access to the object files for the code which is executing on your target system.

Supported compilers

- A compiler which generates object files with the ELF object file format.

Connectors

- You must provide a MICTOR connector, as described in this guide, to connect the logic analyzer probes to the signals on your target system.

Equipment Required

Logic analysis system

You need an Agilent 16900-series or 1680/90-series logic analyzer.

Logic analyzer cards

You need one logic analyzer card. The logic analyzer card must support the speed of the bus you are probing.

Probes

You need a logic analyzer probe (“adapter cable”) to connect the logic analyzer cables to the connector on your target system. The probe must match the type of connector you have placed on your board. Agilent recommends a MICTOR connector and an Agilent E5346A or E5380A probe.

1 Introduction

2 Designing Your Board

This chapter describes the factors you need to consider when designing and preparing your target system for logic analysis.

Overview of the Connectors

Recommended connector

Agilent recommends that you provide one AMP MICTOR 38 connector with the signal mappings shown in the following sections.

Alternative connectors

You are free to use any connector or pin routing, as long as you provide all of the logic analyzer signals that are described for the recommended connector.

If you use a connector or a signal-to-pin mapping other than what is described in this chapter, the Agilent-supplied configuration file will not work. You will need to create your own logic analyzer configuration file. Extreme care must be taken to ensure that your configuration file meets the requirements of the inverse assembler.

- Use a provided configuration file as a model.
- Make sure that your configuration file has the same buses and signals as the provided configuration file. The name and size of each bus and signal must be *exactly* the same as it is in the provided configuration file.
- Verify that all buses and signals listed in the “Buses and signals captured by the logic analyzer” help topic are present.
- Verify that each bus and signal meets all of the requirements specified in this *Design Guide*.

Designing the Connectors

AMP MICTOR 38 connectors

The signal-to-connector mappings shown in this chapter assume you are using an AMP MICTOR 38 connector.

The MICTOR 38 connector carries 32 signals plus two clocks (CLK1 for two logic analyzer pods). A probe (part number E5346A, sometimes called “high-density termination cables”) is required to connect the logic analyzer cables to the MICTOR connector. The probe contains the required termination.

To increase the structural support for the probes, you should use a support shroud on the connector.

For more information, including mechanical dimensions, see the *Agilent Technologies E5346A 38-Pin Probe and E5351A 38-Pin Adapter Cable Installation Note*, available from www.agilent.com.

Design Considerations

The connector must be close enough to the signal source so that the stub length created is less than $^{1}/_{5}$ the t_r (bus risetime). For PC board material, (er = 4.9) and Z_o in the range of 50 - 80Ω, use a propagation delay of 160 ps/inch of stub.

Each probed signal line must be able to supply a minimum of 600 mV to the probe tip and handle a minimum of 90 kΩ shunted by 10 pF. The maximum input voltage to the logic analyzer is ±40V peak

Printed-Circuit Board Design Guidelines

Two cases need to be considered:

- A dedicated trace port. The trace port analyzer is the only load on the trace port signals.
- A shared trace port. The trace pins are shared with other functions; therefore, there are stubs on the printed-circuit board traces of the development board, and there is an increased load on the output driver.

Trace Port

Signal integrity at the trace port analyzer connector is very important. If you know the characteristics of your printed-circuit board traces, use the actual trace impedance and propagation delay.

If you do not have access to this information, a rough rule of thumb for microstrip (trace on outer layer over a ground plane) on FR4 printed-circuit board is a propagation speed of 63 ps/cm (160 ps/inch). The impedance of a 0.127 mm (0.005) inch wide trace as a microstrip is from 70 to 75 Ohms on a typical six-layer foil construction board. The impedance of a trace goes down as the width of the trace increases.

Knowledge of the characteristic impedance and signal edge rates of the FPGA's or ASIC's trace port output drivers is necessary for proper design of the target system. Signals must be carefully routed from the FPGA or ASIC to the trace port connector using high-speed design practices including using termination when necessary.

Also required is the actual setup and hold provided by the trace port outputs with reference to the trace clock. If you do not know the characteristics of the signals from your FPGA or ASIC, consult your vendor. The variation between vendors on trace port output drivers and timing make it difficult to provide any general rule.

Printed-Circuit Board trace Length

Match all TS, ES, D0, BS, and TrcClk trace lengths between the FPGA or ASIC and the trace port connector within 100 ps. Overall differences of greater than 100 ps in trace lengths directly impact setup and hold requirements. If TrcClk is delayed compared to the data, the setup specification needs to be increased by the additional delay. If any data is delayed compared to the clock, the additional delay needs to be added to the setup requirement. If data paths are such that data has both greater than and less than delays compared with the clock, the difference needs to be added to both the setup and hold specification.

Signal Quality

Reflections, overshoot, and undershoot all need to be minimized to ensure accurate data acquisition. The primary variable is the rise time of a signal compared to its trace length. This is where the minimum signal rise and fall time becomes important.

The following points should be considered:

- Ensure the one way propagation time for all traces is less than 1/3 of the signal rise time.
- If traces must be longer than 1/3 of the signal rise time, then some form of signal termination is required. The recommended method is series termination. The series resistor must be placed as close as possible to the FPGA or ASIC pin. The value of this series resistor, when added to the output impedance of the signal driver should closely match the impedance of the printed-circuit board trace. Certain processors include a series resistor in the trace output buffer—see the processor manufacturer's user's guide for details of processor output driver characteristics.
- If series termination cannot be used, add parallel or matched AC termination on each signal trace at the trace port analyzer target connector. This requires significantly more power from the FPGA or ASIC, however, and the AC termination needs to closely match the frequency and rise time of the terminated signal. Therefore, in practice, parallel termination will rarely be possible.
- If the total trace length is one rise time propagation delay or longer in length, follow standard high-speed design practices to minimize cross talk between the clock and the data signals.

NOTE Note that FPGA/ASIC output pads which have an output impedance that is matched to the printed-circuit board trace may be available from your vendor. If these can be used, the signal quality of the trace port signals will be significantly improved.

Signal-To-Connector Mappings

The connector is designed to be used either with an Agilent logic analyzer *or* with a debugger. The signals shaded in blue are for a debugger JTAG controller and are ignored by the logic analyzer. These signals may be safely omitted if the connector will only be used with a logic analyzer.

If you plan to use this connector with a debugger, you must confirm that the JTAG signal locations suggested here are compatible with your JTAG controller. Furthermore, the JTAG signals must be routed to a separate JTAG-only connector so they are accessible to a JTAG controller when the the logic analyzer is connected.

Connections for PPC/MPC 405

Analyzer Pod	Nexus Signal	Mictor pin # (top view)		Nexus Signal	Analyzer Pod
5V	NC	1	2	NC	I2C
5V	NC	3	4	NC	I2C
CLK even	NC	5	6	TrcClk	CLK odd
D15 even	nHALT	7	8	NC	D15 odd
D14 even	nSRESET	9	10	NC	D14 odd
D13 even	TDO	11	12	VTRef	D13 odd
D12 even	NC	13	14	NC	D12 odd
D11 even	TCK	15	16	NC	D11 odd
D10 even	TMS[1]	17	18	NC	D10 odd
D9 even	TDI[1]	19	20	NC	D9 odd
D8 even	nTRST[1]	21	22	NC	D8 odd
D7 even	NC	23	24	TS1o (STATUS - ODD)	D7 odd
D6 even	NC	25	26	TS2o (STATUS - ODD)	D6 odd
D5 even	NC	27	28	TS1e (STATUS - EVEN)	D5 odd
D4 even	NC	29	30	TS2e (STATUS - EVEN)	D4 odd
D3 even	NC	31	32	TS3 (DATA)	D3 odd
D2 even	NC	33	34	TS4 (DATA)	D2 odd
D1 even	NC	35	36	TS5 (DATA)	D1 odd
D0 even	NC	37	38	TS6 (DATA)	D0 odd

Connections for PPC 440

Analyzer Pod	Nexus Signal	Mictor pin # (top view)		Nexus Signal	Analyzer Pod
5V	NC	1	2	NC	I2C
5V	NC	3	4	NC	I2C
CLK even	NC	5	6	TrcClk	CLK odd
D15 even	nHALT	7	8	NC	D15 odd
D14 even	nSRESET	9	10	NC	D14 odd
D13 even	TDO	11	12	VTRef	D13 odd
D12 even	NC	13	14	NC	D12 odd
D11 even	TCK	15	16	NC	D11 odd
D10 even	TMS[1]	17	18	NC	D10 odd
D9 even	TDI[1]	19	20	NC	D9 odd
D8 even	nTRST[1]	21	22	NC	D8 odd
D7 even	D0	23	24	ES4	D7 odd
D6 even	BS0	25	26	TS0	D6 odd
D5 even	BS1	27	28	TS1	D5 odd
D4 even	BS2	29	30	TS2	D4 odd
D3 even	ES0	31	32	TS3	D3 odd
D2 even	ES1	33	34	TS4	D2 odd
D1 even	ES2	35	36	TS5	D1 odd
D0 even	ES3	37	38	TS6	D0 odd

Bus and signal descriptions

NC Pins 1, 2, 3, and 4 must be true no-connects. Other NC signals can be left floating (no connects), or used to measure other signals of interest.

TrcClk Required. Trace clock generated by the target processor.

TS[], ES[], BS[], and D0 Required. These are trace status signals output from the FPGA or ASIC. See IBM's PowerPC 4XX user's guide for details.

Other signals Optional. **The decoder ignores the signals shaded in blue.** These signals are routed to the connector to allow the connector to be used by a JTAG controller. See the documentation for your JTAG controller for information on the requirements for these signals.

In addition, special consideration must be given to these signals so that the logic analyzer does not load them, such that they cannot be controlled by the JTAG controller. Use a 10 kΩ pullup resistor to avoid such loading. See the *Agilent Technologies E5346A 38-Pin Probe and E5351A 38-Pin Adapter Cable Installation Note* for information on how the probe loads the signals.

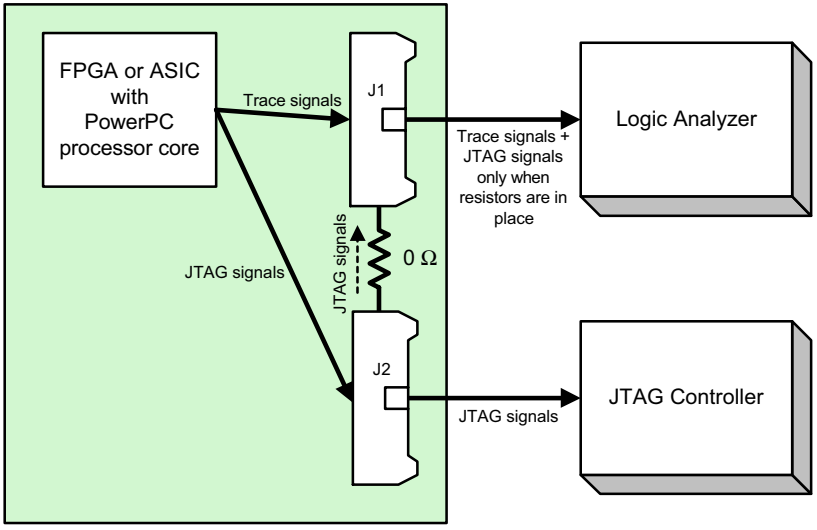
Sharing the Connector Between Multiple Tools

The standard connector defined in this document is designed to be used with a JTAG controller (JTAG run-control with trace) or a logic analyzer (trace only).

There are three possible ways to provide these signals to a JTAG controller and at the same time, prevent the logic analyzer from interfering with their use.

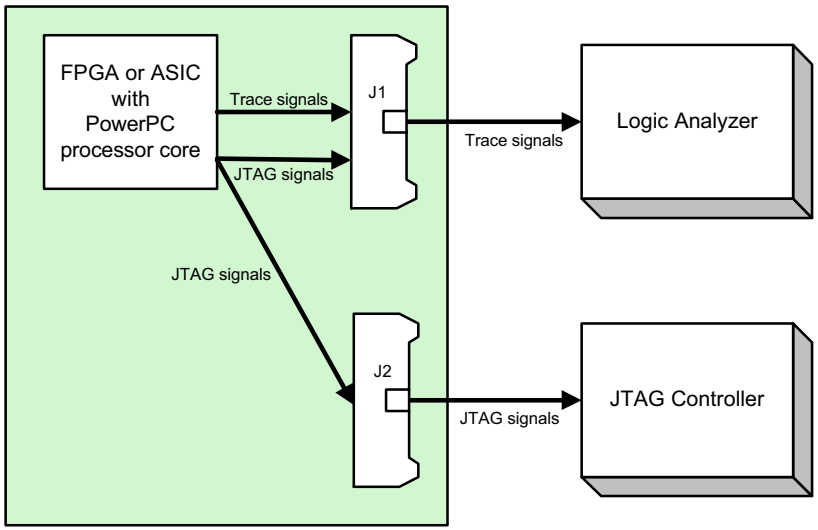
Option 1: Linked connectors

Route the JTAG signals to two connectors on the board. Daisy-chain the signals first to a JTAG-only 2X10 berg connector (J2), then to the MICTOR connector (J1). Place zero-Ohm resistors between the two connectors. Leave the zero-Ohm resistors in place when using J1 with the JTAG controller. Remove the resistors when using J1 with the logic analyzer.



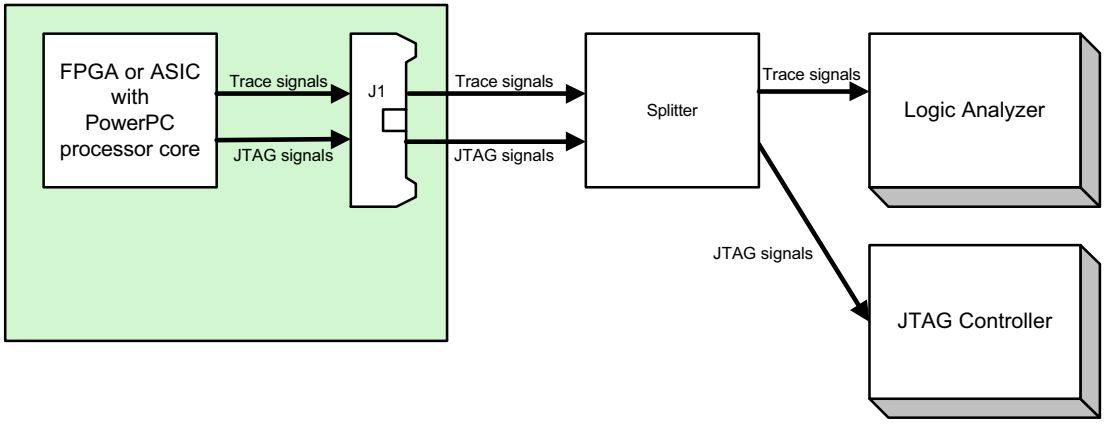
Option 2: Two separate connectors

Route the JTAG signals to two connectors in a star configuration. Provide 10 kΩ pull-up resistors on the signals (particularly nSRST) so that the logic analyzer does not pull these signals to ground.



Option 3: Splitter board

Route the JTAG signals to one connector (J1) and use a splitter board to provide the JTAG-only connector for the JTAG controller. You will need to supply your own splitter board.



Index

Index